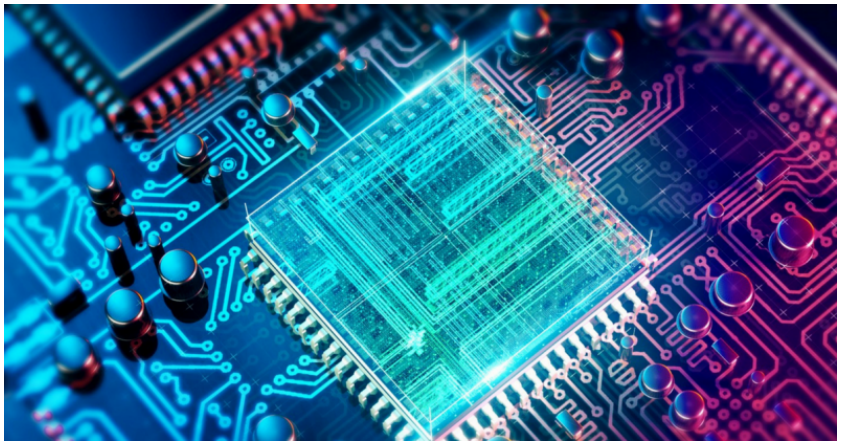
High-Performance Computing with FPGAs and OpenCL



FPGAs are one of the accelerators that are recently emerging as more power-efficient alternatives to GPUs in world-class supercomputers. In particularly, FPGAs excel at stencil computations.

This work focus on implementing a subset of the *Rodinia* benchmark suite for these type of applications. We take advantage of High-Level Synthesis (HLS) that allows FPGAs to be easily programmed in software languages, such as C++,, OpenCL. Thereby, we target Intel and Xilinx FPGAs.

We aim to develop an open source library, where FPGA-specific optimizations are hidden to the user. We will benchmark our implementations on state-of-the-art FPGAs that can be accessed in the cloud servers (i.e. Amazon AWS).

The main tasks are:
a) investigating FPGA/HLS design techniques for Rodinia benchmark
b) developing a template-based library for high-performance computing
c) benchmarking the target applications on cloud servers

Required skills:	Self-Learning, Enthusiasm on Research, C++, and Understanding of FPGA design
Nature of work:	Theory (30 %), Conception (30 %), Implementation (40 %)
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design

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