A DSL for Image Processing

**HIPA**: The Heterogeneous Image Processing Acceleration Framework

**HIPA** Classes

- **Image**
  - input/output buffers
- **Accessor**
  - ROI of input image
  - boundary handling
  - interpolation/filtering
- **IterationSpace**
  - ROI of output image
  - compute kernel description
- **Mask**
  - convolution mask
- **Domain**
  - iteration domain
- **Pyramid**
  - image pyramid description

**Domain Knowledge**

- LUT
- FF
- BRAM
- DSP
- HC
- LP3D
- LP5
- HC3
- OF
- GPU
- HLS
- OpenCL
- C++
- HLS
- Vivado
- RTL
- C++
- C++
- HDL
- HIPA

**Trace and Analyze DSL Code**

- allocation of buffers
- data transfers
- kernel executions with data dependencies
- build up dependency graph
- identify memory reuse
- translate to internal representation

**Internal Representation**

Use internal representation to transform the execution order of HIPA kernels into a pipelined and streamed execution:

- model as a combination of spaces and processes to describe the pipeline
- insert copy processes for multiple kernels reading the same buffer
- prune dead code by traversing in depth-first search starting from output spaces

**Generating the Streaming Pipeline**

- infer structural description from spaces and processes
- create unique stream for each space
- insert generated kernel code for non-copy processes
- read single value from input stream and propagate to multiple output streams

**Kernel Code Generation**

- single line buffer in BRAM
- single window buffer in reg.
- pack vector channels into wider stream type (e.g., uint32_t, ...)
- only use single window and line buffer for all channels
- apply vector operations by operator overloading

**Results**

**Throughput: OpenCV vs. HIPA**

- increasing algorithm complexity decreases throughput
- faster than Xilinx OpenCV
- Harris Corner (HC) twice as fast
- OpenCV $H = 2$
- HIPA $H = 1$

**Resource Costs: OpenCV vs. HIPA**

- lower overall resource cost
- higher achievable frequency
- comparable results for Harris Corner (HC) but twice as fast

**Targets: GPUs vs. FPGAs**

- GPUs suffer dramatically from number of memory accesses
- FPGA latency is almost solely dependent on image size
- ARM Mali T604 suffers from register spilling for Optical Flow (OF)

**Selected Publications**


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**Figure 1: Overview of the HIPA Framework**

**Figure 2: Harris Corner detector as sequential HIPA execution of kernels using host barriers**

**Figure 3: Internal representation of the Harris Corner detector provided for Vivado**

**Figure 4: Line buffer and group delay**

**Figure 5: Pack multiple vector channels into single stream**

**Figure 6: Throughput comparison**

**Figure 7: Resource cost comparison**

**Figure 8: Multiple implementations stemming from the exact same code base**