Second International Workshop on

FPGAs for Software Programmers (FSP 2015)

September 1, 2015, London, United Kingdom

Program

9:00 - 9:10  Welcome and Introduction  Dirk Koch, Tobias Becker, Frank Hannig, and Daniel Ziener

9:10 - 10:10  Keynote Speech 1

9:10 - 10:10  Application Acceleration with the VectorBlox MXP  Guy Lemieux, Founder, CEO, and CTO of VectorBlox Computing Inc.

10:10 - 10:30  Fast-Forward Presentation of Posters

P1: OpenCL 2.0 for FPGAs using OCLAcc  Franz Richter-Gottfried, Alexander Ditter, and Dietmar Fey

P2: Proposal of ROS-compliant FPGA Component for Low-Power Robotic Systems  Kazushi Yamashina, Takeshi Ohkawa, Kanemitsu Ootsu, and Takashi Yokota

P3: Performance Monitoring for Multicore Embedded Computing Systems on FPGAs  Lesley Shannon, Eric Matthews, Nicholas Doyle, and Alexandra Fedorova


P5: A Comparison of High-Level Design Tools for SoC-FPGA on Disparity Map Calculation Example  Shaodong Qin and Maden Berekovic

P6: RIPL: An Efficient Image Processing DSL for FPGAs  Robert Stewart, Deepayan Bhowmik, Greg Michaelson, and Andrew Wallace

P7: GCC-Plugin for Automated Accelerator Generation and Integration on Hybrid FPGA-SoCs  Markus Vogt, Gerald Hempel, Jeronimo Castrillon, and Christian Hochberger

P8: Using System Hyper Pipelining (SHP) to improve the Performance of a Coarse-Grained Reconfigurable Architecture (CGRA) Mapped on an FPGA  Tobias Strauch

P9: Transparent Hardware Synthesis of Java for Predictable Large-Scale Distributed Systems  Ian Gray, Yu Chan, Jamie Garside, Neil Audsley, and Andy Wellings

10:30 - 11:00  Coffee Break and Posters

11:00 - 12:30  Session 1: HLS Tooling  Chair: Frank Hannig

11:00 - 11:22  Allowing Software Developers to Debug HLS Hardware  jeffrey Goeders and Steve J. E. Wilton

11:23 - 11:45  Model-based Hardware Design for FPGAs using Folding Transformations based on Subcircuits  Konrad Möller, Martin Kunnm, Charles-Frederic Müller, and Peter Zipf

11:45 - 12:07  Automatic Nested Loop Acceleration on FPGAs Using Soft CGRA Overlay  Cheng Liu, Ho-Cheung Ng, and Hayden Kwok-Hay So

12:08 - 12:30  ThreadPoolComposer – An Open-Source FPGA Toolchain for Software Developers  Jens Korinith, David de la Chevalerie, and Andreas Koch

12:30 - 13:30  Lunch

13:30 - 14:30  Keynote Speech 2

13:30 - 14:30  Porting of a Particle Transport Code to an FPGA  Iakovos Panourgias, EPCC, University of Edinburgh

14:30 - 15:00  Session 2: Mapping for Stream Processing Applications  Chair: Tobias Becker

14:30 - 14:45  Framework for Application Mapping over Packet-switched Network of FPGAs: Case studies  Vinay B. Y. Kumar, Pinalkumar Engineer, Mandar Datar, Yatis Turakhia, Saurabh Agarwal, Sanket Diwale, and Sachin B. Patkar

14:45 - 15:00  DSL-based Design Space Exploration for Temporal and Spatial Parallelism of Custom Stream Computing  Kentaro Sano

15:00 - 15:30  Coffee Break

15:30 - 17:00  Session 3: Heterogeneous Computing – From Embedded to Cloud  Chair: George Constantinides


15:53 - 16:15  Designing Hardware/Software Systems for Embedded High-Performance Computing  Mário P. Véstias, Rui Policarpo Duarte, and Horácio C. Neto

16:15 - 16:37  RCSE: Provision and Management of Reconfigurable Hardware Accelerators in a Cloud Environment  Oliver Knodel and Rainer G. Spailek

16:38 - 17:00  Seeing Shapes in Clouds: On the Performance-Cost Trade-Off for Heterogeneous Infrastructure-as-a-Service  Gordon Inggs, David B. Thomas, George Constantinides, and Wayne Luk

17:00  Closing

Co-Organizers:
Tobias Becker, Maxeler Technologies
Frank Hannig, Friedrich-Alexander University Erlangen-Nürnberg (FAU)
Dirk Koch, University of Manchester
Daniel Ziener, Friedrich-Alexander University Erlangen-Nürnberg (FAU)

Technical Program Committee:
Hitoshi Amano, Kao University, Japan
Jason H. Andersen, University of Toronto, Canada
Gordon Bradner, Xilinx Inc., USA
Jude M. P. Cardoso, University of Porto, Portugal
Sunita Chandrasekaran, Univ. of Houston, USA
Andreas Koch, TU Darmstadt, Germany
Miriam Lesser, Northwestern University, USA
Waldid Najjar, University of California Riverside, USA
Gael Paul, PLDA, France
Marco Platzner, University of Paderborn, Germany
Dan Poznanovic, Cray Inc., USA
Rodric Rabbah, IBM Research, USA
Olivier Sentieys, University of Rennes, France

Dirk Stroobandt, Ghent University, Belgium
Gustavo Sutter, Autonomous University of Madrid, Spain
David Thomas, Imperial College London, UK
Kazutoshi Wakabayashi, NEC Corp., Japan
Markus Weinhard, Osnabrück Univ. of Appl. S., Germany
Peter Yiannacouras, Altera Corp., Canada